REMARKS

Claims 1-22 are pending in the current application. Claims 1, 16, 20, 21 and 22 are independent claims. No new matter has been added. Favorable reconsideration in view of the following remarks is respectfully requested.

35 U.S.C. § 112, SECOND PARAGRAPH

Claims 1-19 and 21 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Applicant respectfully traverses.

With regard to the first and/or second conductors recited in claims 1, 16, 21 and 22, Applicant submits that the conductors may be bonding wires according to example embodiments of the present invention. Applicant directs the Examiner's attention, for example, to paragraph [0025] of the Specification or dependent claim 15. Thus, the conductive element is not missing.

Further, claims 1, 4, 16 and 21 have been amended to include the proper antecedent basis.

Thus, the rejection has been overcome. Reconsideration and withdrawal is respectfully requested.

35 U.S.C. § 102 (e) REJECTION – HABA

Claims 1, 2, 6, 7, 16, 17, 19 and 21 remain rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by Haba et al. (hereinafter 'Haba'), U.S. Patent No. 6,376,904. Applicant respectfully traverses this rejection.

Relying on FIG. 13 of Haba, reproduced below in color, the Examiner asserts that the semiconductor chips 1312/1314 (red) and the lower bottom chip (purple) under 1312/1314 (but not labeled) read on the first and second semiconductor chips, respectively, as recited in independent claim 1. Further, the Examiner asserts that the "...conductor wires and electrode pad electrically extending from the lower bottom chip under 1312 but not labeled electrically connecting to the pad on 420..." read on "...electrically connecting the second semiconductor chip to the frame..." Action, p. 4. Applicant disagrees.

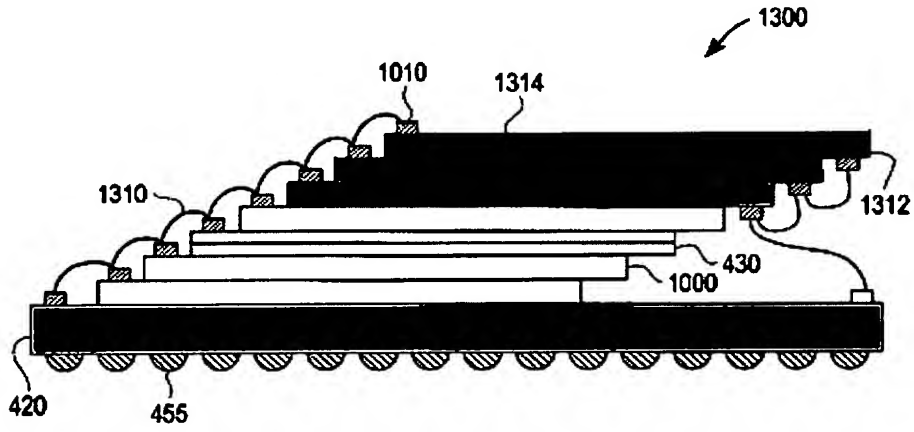

FIG. 13 of Haba

Assuming *arguendo* that the Examiner's assertion is correct, which Applicant does not agree, Haba teaches that the second chip (purple) is **under**, not over, the first chip (red). Furthermore, an intermediate chip (green) would be connected to the base 420 (orange), not the topmost chip (red) (as recited in independent claims 1 and 21 of the present invention) or the second chip (purple) (as suggested by the Examiner). Thus, Haba fails to teach all of the limitations of independent claims 1 and 21.

As such, Applicant submits that Haba fails to suggest or anticipate "a second semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed and at least one bottom corner of the second

semiconductor chip is exposed" and "at least one second conductor electrically connecting the second semiconductor chip to a frame" as recited in independent claim 1, and similarly recited in independent claim 21.

Reconsideration and withdrawal of the rejection to independent claims 1 and 21 is respectfully requested.

Accordingly, Applicant kindly requests reconsideration and withdrawal of the rejection to claims 2, 6, 7 and 19, at least by virtue of their dependency on independent claim 1.

With regard to independent claim 16, the Examiner asserts that Haba teaches the limitations of claim 16. Applicant disagrees.

Applicant submits that independent claim 16 recites a limitation wherein each intermediate semiconductor chip stacked offset over the first semiconductor chip; and a second conductor is stacked offset over the intermediate chips such that at least one bottom corner of the second semiconductor chip is exposed.

Thus, for similar reasons as given above, Haba also fails to anticipate or suggest "a second semiconductor chip, wherein when the expression $n > 0$ is satisfied, the second semiconductor chip is stacked offset over the intermediate semiconductor chips such that a portion of each intermediate semiconductor chip and at least one bottom corner of the second semiconductor chip are exposed" and "at least one second conductor electrically connecting the second semiconductor chip to a frame" as recited in independent claim 16.

Reconsideration and withdrawal of the rejection to independent claim 16, and claim 17 by virtue of its dependency on independent claim 16, is respectfully requested.

35 U.S.C. § 102 (e) REJECTION – VERMA

Claims 1, 2, 6-8, 16, 17, 19 and 21 stand rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by Verma et al. (hereinafter "Verma"), U.S. Patent Publication No. 2003/0155659. Applicant traverses.

Verma, directed to a memory module formed including two or more stacked integrated circuits mounted to a substrate or lead frame, teaches a stacked configuration with "the capability to utilize bonding pads on all four sides of an integrated circuit." Verma, Abstract. A cross sectional view of the memory module 60, shown in FIG. 6 (reproduced below), illustrates that the sides on the upper surface of the storage element 40b are exposed, as well as, the sides on the upper surface of the controller 40a.

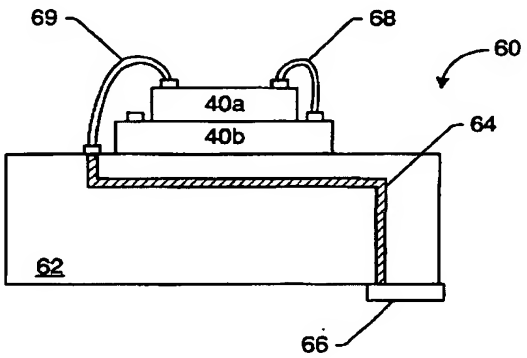

FIG. 6 of Verma

Because all four sides on the upper surface of the storage element 406 are used, the controller 40a does not offset, or hang over, the storage element 40b such that any of the bottom corners of controller 40a are exposed.

Thus, Verma fails to teach that the controller 40a is stacked offset such that at least one bottom corner of the controller 40a is exposed. As such, Verma fails to teach all of the limitations of amended independent claims 1 and 21.

Accordingly, Applicant submits that Verma fails to anticipate or suggest "a second semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed and at least one bottom corner of the second semiconductor chip is exposed" as recited in independent claim 1, and similarly recited in independent claim 21.

Reconsideration and withdrawal of the rejection to independent claims 1 and 21 is respectfully requested.

Applicant kindly requests reconsideration and withdrawal of the rejection to claims 2, 6-8 and 19, at least by virtue of their dependency on independent claim 1.

With regard to independent claim 16, the Examiner asserts that Verma teaches the limitations of claim 16. Applicant disagrees.

Applicant submits that independent claim 16 recites a limitation wherein at least one bottom corner of the second semiconductor chip is exposed.

Thus, for similar reasons as given above, Verma also fails to anticipate or suggest "a second semiconductor chip, wherein when the expression $n > 0$ is satisfied, the second semiconductor chip is stacked offset over the intermediate semiconductor chips such that a portion of each intermediate semiconductor chip and at least one bottom corner of the second semiconductor chip are exposed, and when the expression $n = 0$ is satisfied, the second semiconductor chip is stacked offset over the first semiconductor chip such that the portion of the first semiconductor chip and the at least one bottom corner of the second semiconductor chip are exposed" as recited in independent claim 16.

Reconsideration and withdrawal of the rejection to independent claim 16, and claim 17 by virtue of its dependency on independent claim 16, is respectfully requested.

35 U.S.C. § 102 (e) REJECTION – KATO

Claims 1-22 stand rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by Kato et al. (hereinafter "Kato"), U.S. Patent Publication No. 2002/0140107 A1. Applicant traverses this rejection.

With regard to independent claims 1 and 21, Kato teaches stacking the second semiconductor chip 12A on top of the first semiconductor chip 11A wherein "...of the first semiconductor chip and the second semiconductor chip, the semiconductor chip with the larger area is disposed at a lower layer with respect to a direction of stacking." Kato, paragraph [0030]. Applicant directs the Examiner's attention to FIGs. 1 and 2, which depict a cross-sectional and plan view, respectively, of semiconductor device 10A. Semiconductor device 10A includes the semiconductor chip 12A stacked on top of the semiconductor chip 11A wherein "[t]he first alignment mark 22 is used when stacking the second semiconductor chip 12A on the first semiconductor chip 11A in order to carry out positioning of the chips 11A, 12A." Kato, paragraph [0175]. The first alignment marks 22 (located at opposite corners) are positioned within the parameters of the first semiconductor chip 11A such that the surface area of the second semiconductor chip's upper surface is less than the surface area of the first semiconductor chip's upper surface. Therefore, the sides on the upper surface of each semiconductor chip are exposed. Thus, similar to Verma, the configuration prevents the bottom corners of the second semiconductor chip 12A from being exposed.

Therefore, Kato fails to teach that the second semiconductor is stacked offset such that at least one bottom corner of the second semiconductor is exposed. Thus, Kato also fails to teach all of the limitations of amended independent claims 1 and 21.

As such, Applicant submits that Kato fails to anticipate or suggest "a second semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed and at least one bottom corner of the second semiconductor is exposed" as recited in independent claim 1, and similarly recited in independent claim 21.

Reconsideration and withdrawal of the rejection to independent claims 1 and 21 is respectfully requested.

Accordingly, Applicant kindly requests reconsideration and withdrawal of the rejection to claims 2-15, 18 and 19 at least by virtue of their dependency on independent claim 1.

With regard to independent claims 16, 20 and 22, Applicant submits that independent claims 16, 20 and 22 recite a similar limitation to that, argued above, in independent claims 1 and 21.

Thus, for similar reasons as given above, Kato also fails to anticipate or suggest "a second semiconductor chip, wherein when the expression $n > 0$ is satisfied, the second semiconductor chip is stacked offset over the intermediate semiconductor chips such that a portion of each intermediate semiconductor chip and at least one bottom corner of the second semiconductor chip are exposed, and when the expression $n = 0$ is satisfied, the second semiconductor chip is stacked offset over the first semiconductor chip such that the portion of

the first semiconductor chip and the at least one bottom corner of the second semiconductor chip are exposed" as recited in independent claim 16.

Kato also fails to anticipate or suggest "a stacked chip structure including an upper semiconductor chip and at least one lower semiconductor chip disposed under at least a portion of the upper semiconductor chip such that at least one bottom corner of the upper semiconductor is exposed" as recited in independent claims 20 and 22.

Accordingly, reconsideration and withdrawal of the rejection to independent claims 16, 20 and 22 is respectfully requested.

Applicant respectfully requests that the Examiner reconsider and withdraw the rejection to claim 17, at least by virtue of its depending on independent claim 16.

CONCLUSION

Accordingly, in view of the above, reconsideration of the rejections and allowance of the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) hereby petition(s) for a one (1) month extension of time for filing a reply to the outstanding Office Action and submit the required $120.00 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____
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